DSP-FPGA BASED EFFICIENT AND CONTROLLED BRAKING METHOD FOR MULTILEVEL MEDIUM VOLTAGE INDUCTION MOTOR DRIVE

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ABSTRACT: Any variable frequency drive requires an efficient and controlled braking system. Therefore, different braking techniques have been the subject area of researchers to enhance the performance as well as overall life of the drives. In this paper, a literature study is made of various existing braking methods, focused on induction motor (IM) drive performance. The braking methods are compared and summarized based on speed range, braking time and efficiency of 13 level medium voltage 3-phase squirrel cage IM drive. Finally, an advanced D.C. braking technique is presented where braking torque in terms of varying D.C. signal is injected into the stator windings using fully controlled phase shifted carrier sine pulse Width Modulation (PSC-SPWM). A method has been described for providing occasional fast, smooth and controlled braking torque from a non-regenerative VFD, without additional power circuits. Simulations are performed in MATLAB/Simulink, tested and validated on Digital signal processor (DSP) and Field-Programmable Gate Array (FPGA) based drive. Control algorithm written in DSP and FPGA, is used to generate PWM signals because it is fast, having simple hardware and software design. Test results are presented in this paper.

KEYWORDS: 3-Phase Induction Motor, Braking, Conventional, MATLAB/Simulink, DSP, MATLAB, FPGA, 13 Level medium Drive.

INTRODUCTION

Three-phase induction motor drives are extensively used in different sectors of drives industry, but it is a challenge to stop them in short period of time especially for high inertia loads. To control an electric machine by electric drives, its braking system is very important because it helps to decrease the speed of the motor according to will and necessity. Braking is also a part of controlled stopping (as opposed to coasting), which helps to increase occupational safety while reducing wear on power transmission belts, sprockets, and gears. Besides mechanical brakes, today's options include electronic brakes.

Electronic D.C. braking provides reliable and fast load deceleration and stopping, requiring no maintenance and conserves energy as well with reduced maintenance costs. Many such applications where D.C. injection braking can be deployed are roller-table drives, grinding machines, centrifuges, circular saws, planers, roller and ball mills and so on to cut down stopping time. D.C. braking reduces undesirable oscillations and even vibratory motors can be stopped within few tens of seconds. Apart from all these, D.C. braking increases safety and productivity at the same time. Many conventional braking schemes are already practiced by leading industrial drive manufacturers which could be broadly classified into two parts VFD and Non-VFD based braking. Non-VFD braking includes capacitor self-excitation braking, electronic brake module using rectifiers and thyristors for D.C. injection, single short circuit method (magnetic braking), simultaneous magnetic braking and D.C. injection [6], zero sequence braking, etc. VFD braking includes flux braking, dynamic braking (like D.C. injection braking, regenerative braking), double frequency braking, etc.

Recently researchers and industrial companies have put their special interest in multilevel inverters (MLI). MLI generates nearly sinusoidal voltage with very low distortion and it also reduces dv/dt stresses, producing smaller common voltage and reduced stress in the bearings of a motor. MLI draws input current with low distortion. It reduces switching losses.

MULTILEVEL CONVERTER TOPOLOGIES

Multilevel converters are a new breed of converter topologies that have drawn much attention since last decade for their advantage of delivering increased power level. Moreover, there is a freedom in applying modulation strategy in case of multilevel inverters to improve their performance. Mainly three types of multilevel converter topologies are being followed in research as well as industry level [8]. For 5-level converter those are as follows:

Table 2.1. Components required in three topologies

	Diode Clamped	Flying-Capacitor	Cascaded-Cell
Transistor	24	24	24
Clamping Diode	132	0	0
D.C. Bus Capacitor	12	12	6

Neutral-Point Clamped or Diode-Clamped

This type of converter topology uses clamped diodes and D.C. capacitors in order to generate multilevel AC voltage.

Flying-Capacitor

In this topology, semiconductor switches are in series and their connecting points are clamped by extra capacitors.

Cascaded H-bridge

This topology of multilevel converter comprises of several H-bridge cells (Full-bridge Voltage source inverters) connected in series. Comparison has made among these three topologies on the basis of components required and listed in table 1.

SWITCHING STRATEGY

The switching methods in multilevel inverter are one of the significant areas of research at present. This is due to the fact that the adopted switching technique has a great impact on the harmonic content of the produced AC waveform. Also, the switching losses are also directly dependent on the switching algorithm. In case of multilevel converters, three types of switching schemes are usually followed:

- **Selective Harmonic Elimination**

In this method, each switch is turned on and turned off once in a switching cycle and switching angles are usually chosen based on specific harmonics elimination or minimization of output voltage Total Harmonic Distortion (THD).

- **Carrier based PWM**

This switching scheme produces gate signals for semiconductor switches by comparison of a reference (modulating) signal with a carrier signal.

- **Space Vector PWM**

In this method, a reference voltage vector is constructed with the help of switching space vectors within a sample period.

Modulation Technique of Carrier Based PWM

The modulation technique of carrier based PWM can be broadly classified into two categories as listed below:

- *Phase-shifted carrier based PWM:* Multilevel inverter with ‘m’ levels requires ‘(m-1)’ triangular carrier signals. In this kind of modulation, all the triangular carriers have the same frequency and same amplitude, but there is a phase shift between any two adjacent carrier signals, given by Eqn. 1.

$$\varphi_{cr} = \frac{360}{m-1} \qquad (1)$$

The amplitude modulation index in Eqn. 2.

$$ma = {}^{U_m}/_{U_{cr}} \tag{2}$$

U_m is the peak amplitude of the modulating signal and U_{cr} is the peak amplitude of each carrier signal.
Fig. 1 shows modulating signal and a carrier wave of 750Hz. Such 12 phase shifted carriers are compared with modulating signal to create 12 PWMs as shown. These 12 PWMs are complimented by NOT gate. Such 24 PWMs are then given to one leg of cascaded H-bridge which ultimately generates multilevel voltage waveform. The line-to-line voltage and line to neutral voltage waveform is shown in Fig. 2.

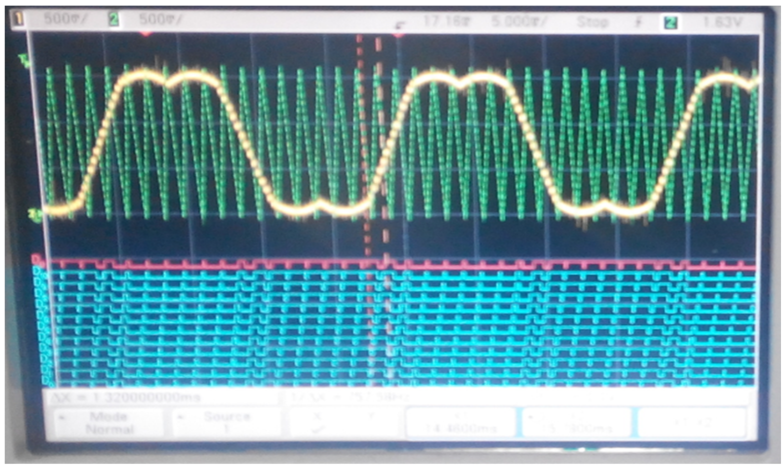

Figure 1. Modulating signal, carrier wave and 12 PWMs for single leg

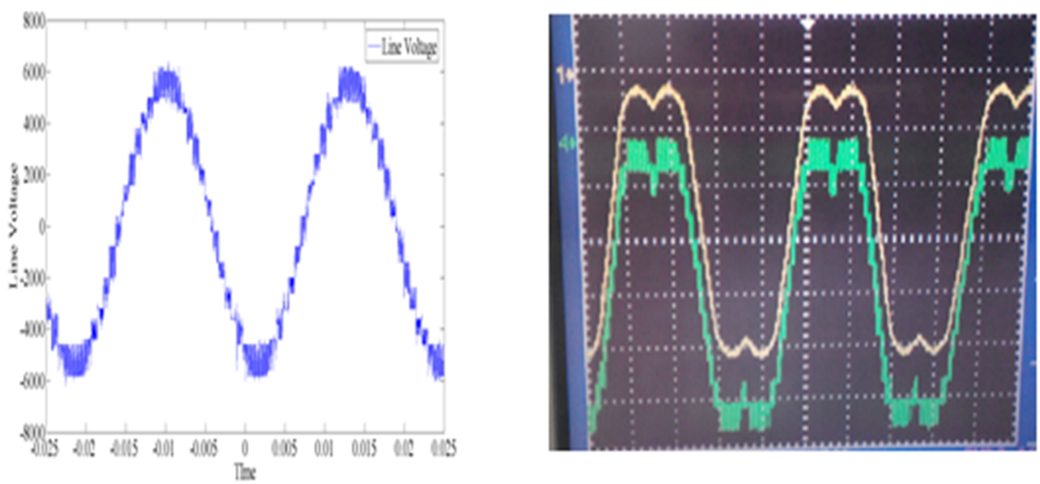

Figure 2. 13 level line-to-line multilevel voltage and phase to neutral voltage

- *Level-shifted carrier based PWM:* In case of level shifted carrier, the triangular carriers have the same frequency and amplitude like that of the phase shifted carriers. But the difference lies in the modulation index as given by:

$$m_a = \frac{U_m}{U_{cr}(m-1)} \qquad \text{for } 0 \le m_a \le 1 \tag{3}$$

CONTROLLED BRAKING SCHEME

In VFD based D.C Injection, the amount of braking torque depends on the magnitude of the current which can be varied pulse by pulse. This allows the retardation to be varied over a wide time range. D.C. braking is initiated following a brakeenable delay of approx. 200ms. As soon as the set braking time-out is reached the PWM pulses are inhibited and the braking current decays. A typical torque-speed curve for braking of a cage motor is shown in Fig.3, from which we see that the braking (negative) torque falls to zero as the rotor comes to rest. Braking is a dissipative process, all the kinetic energy being turned into heat inside the motor. For standard D.C. braking method (VFD based) braking torque can be generated only up to 66% whereas proposed advanced D.C. braking is capable of generating braking torque up to 100%.

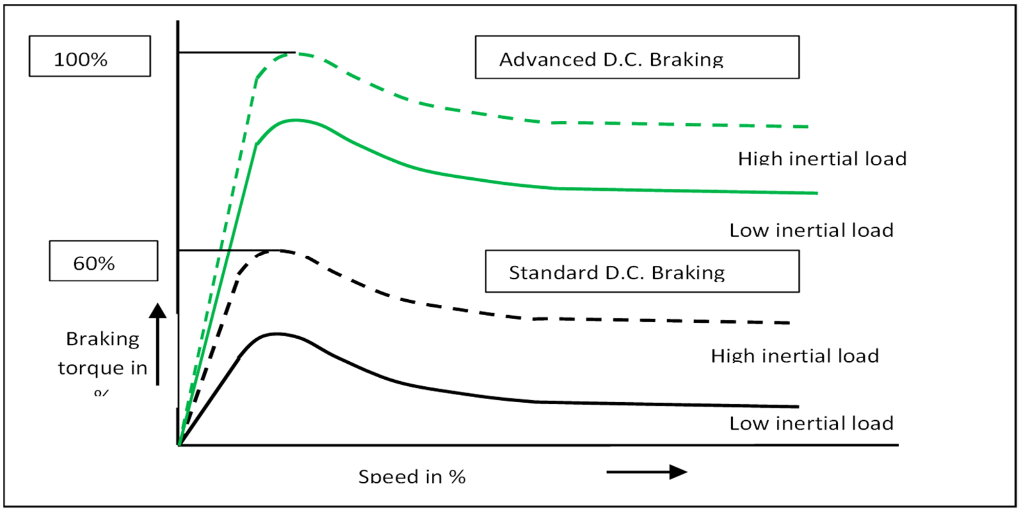

Figure 3. Torque Speed Curve of IM

Characteristic of dynamic braking (fast ramp down) is the typical nonlinear stopping characteristic as shown in Fig.4. To increase the deceleration rate (decrease the stopping time), D.C. can be applied to the motor windings during the last 10% to 20% of the motor's speed. For example, a motor is turning at 1,500 rpm when the stop command is issued. Fast deceleration ramp reduces the speed to 150 rpm, and then injecting D.C. reduces the total stopping time by many seconds than if it were stop only by dynamic braking alone.

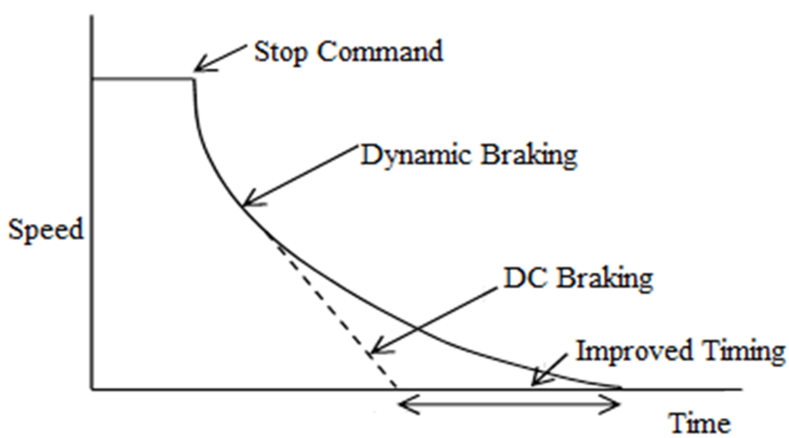

Figure 4. Stopping with dynamic braking and D.C. injection braking

PROPOSED MODIFIED D.C. INJECTION

In this paper cascaded H-Bridge MLI is used with phase shifted carrier Sine PWM technique. Fig.5 shows line to line voltage, line current and one cell voltage.

VFDs have always included cost effective methods for providing fast, reliable braking. In this paper, an advanced technique of D.C. injection has been proposed that is flexible and easy to implement. The disadvantage of traditional D.C. injection is that maximum braking torque is limited (approximately 66% of full motor torque) and motor heating can be excessive. Dynamic braking uses a resistor bank to dissipate the heat. The motor being decelerated operate as a generator, which feeds energy into the drive's D.C. bus and braking resistor.

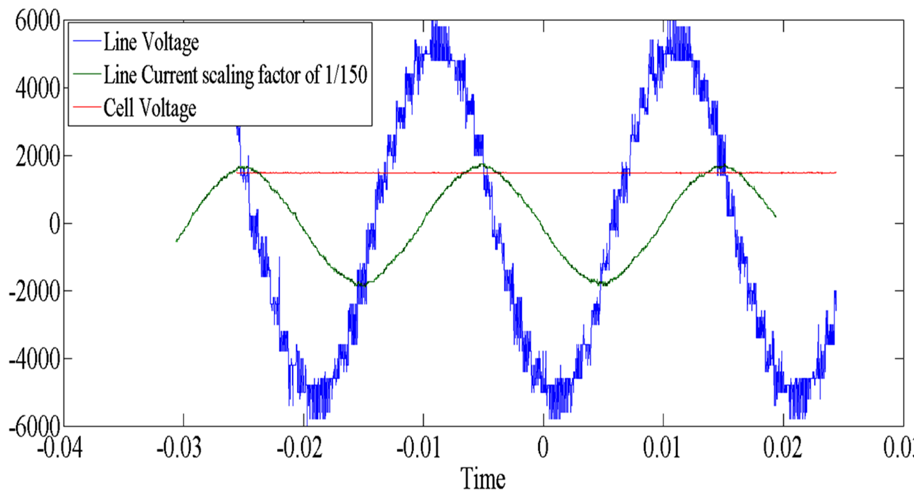

Figure 5. Output voltage, current and cell voltage waveform for 13 level inverter

When braking is in progress, the frequency of voltage is controlled to maintain negative slip. This allows kinetic energy to be absorbed from the motor and load inertia. Voltage is applied to dissipate the absorbed energy in the motor as heat. Fig.6 illustrates the balance of energy during braking.

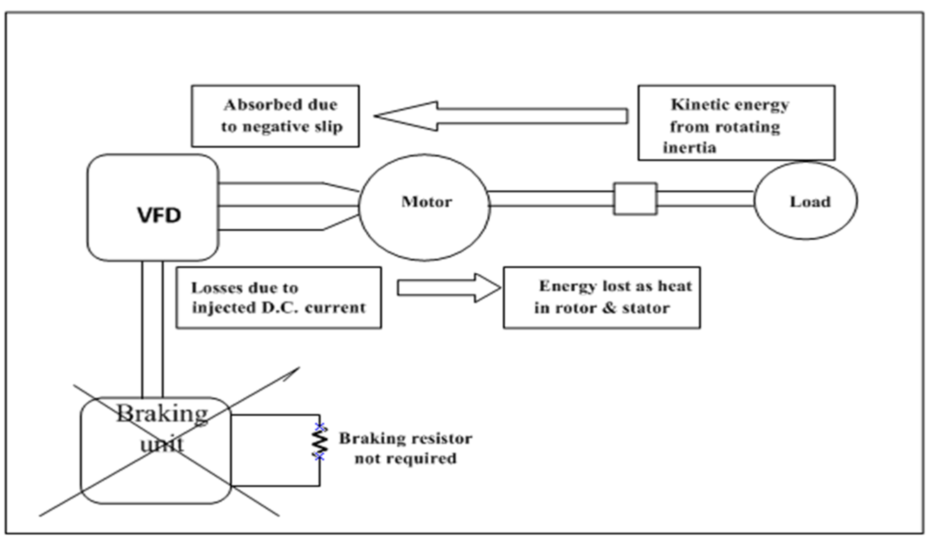

Figure 6. Balance of energy during D.C. braking

Proposed advance D.C. Breaking is a cost-effective sopping method, produces drastic reduction in braking time while eliminating the need for an expense of external braking resistors and additional braking chopper power circuits by offering higher braking torque per ampere in non-regenerative ac drives. The modified D.C. braking discussed in this paper for high inertia loads can provide braking torque in excess of 100% full load motor torque. Control scheme, controls the deceleration to make the motor operate as very inefficient induction generator by modifying the V/F pattern so that load energy is observed in the rotor bars, stator windings and stator core of the motor. Current level is controlled to avoid excessive motor heating. Deceleration time is directly related to the actual load torque and inertia.
Simulations are performed on MATLAB/Simulink platform (R2014a) as in Fig. 7.

Here D.C., in form of pulses is injected in two phases and magnetic braking is performed by shorting two phases externally. Three phases and single phase switches are used to switch the braking methods using specified time. Series of experiments were performed and graphs were plotted to analyze the results.
To apply D.C. braking, duty cycle of PWM pulses were varied based on current required denoted in Eqn. 4 and Eqn. 5.

$$\frac{\frac{T_{on}}{T} * V_{DC}}{2R_s} = I_{req} \qquad (4)$$

$$\frac{T_{on}}{T} = \frac{2R_s * I_{req}}{V_{DC}} \quad (5)$$

I_{req} is the required D.C. current to be injected. T_{ON} is the ON time of the injected pulses. R_s is the stator resistance, V_{DC} is the D.C. bus voltage.

MATLAB SIMULATION RESULT

To apply D.C. braking we have two methods, one is to apply D.C. after supply is cut-off and base-block time is attained. And in second method motor speed is decelerated according to deceleration ramp in 'ramp to stop' and when speed reaches pre-determined value D.C. braking is applied. The amplitude of D.C. Braking current affects the strength of the braking torque attempting to lock the motor shaft. Increasing the level of current increases the amount of heat generated in stator windings.

Referring Fig.8, The control strategy used for simulation is constant V/Hz method in which RPM is taken as input is converted in frequency as, $freq = speed * p/120$, where p is number of poles. The frequency is taken as reference and corresponding modulation index is selected by constant V/Hz curve. Pulses are generated by phase shifted carrier SPWM and applied to converter. Converter generates three phase AC signals and these signals are fed to motor via circuit breaker. Loads ranging from 0 to full are selected by switch. Second circuit breaker is used for applying D.C. Braking. Line voltage, stator current, speed and motor torque were observed in scope. Induction motor was stopped at $t = 5sec$, and D.C. Braking applied after $t = 5.7sec$ as shown in Fig. 8.

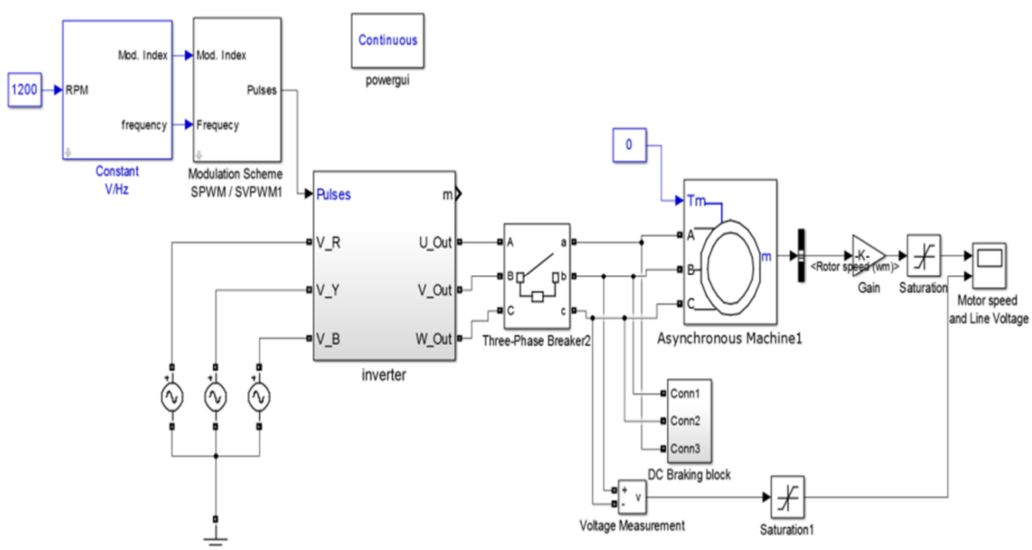

Figure 7. MATLAB circuit of D.C. injection braking

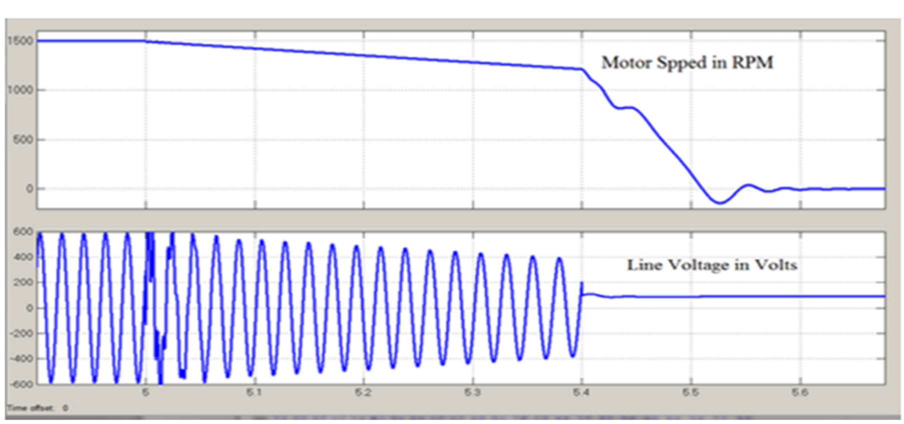

Figure 8. Speed-time curve and line to line voltage when DC braking is applied

- *DSP*: The control of the IM drive in actual hardware set-up is carried out through Digital Signal Processor (DSP). TMS320F28335 is used for the purpose, TMS320F28335 is MCU based control-CARD by Texas instruments having High-Performance Static CMOS Technology and clock frequency of 150MHz. TMS320F28335 is single-precision floating point DSP having 32 bit CPU. TMS320F28335 having six-channel DMA controller for ADC, ePWM. This DSP is well suited for motor control applications.
- *FPGA:* The Spartan 3E Starter Board provides a powerful and highly advanced self-contained development platform for designs targeting the Spartan 3E FPGA from Xilinx. It features a 500K gate Spartan 3E FPGA with a 32 bit RISC processor and DDR interfaces. It has 100-pin Hirose FX2 connector, three 6-pin Pmod connectors, DB15HD VGA connector, Two DB9 RS-232 connectors, RJ-45 Ethernet connector, 16-pin header for optional LCD modules and SMA connector for high-speed clock input. The board also features a Xilinx Platform Flash, USB and JTAG parallel programming interfaces with numerous FPGA configuration options via the onboard Intel StrataFlash and ST Microelectronics Serial Flash.
- *Hardware Setup Result:* Applying D.C. in two phases in terms of fixed duty cycle pulses is not feasible as sufficient back emf appears in off period and as a result average D.C. is low [9]. Hence, this paper proposes a technique where very low frequency of 1/100Hz sine wave with less modulation index of 0.2 is applied for the time duration of 200msec for each phase. For such small time the sine wave can be approximated as D.C. signal and the problem of back emf can be avoided.

The complete block diagram of MLI is shown in fig.9. The control algorithm viz V/F control, ramp control etc. are written in DSP while FPGA is used to compare modulating signals with triangular waves to generate PWMs. Serial Peripheral Interface (SPI) protocol is used to communicate in-between DSP and FPGA.

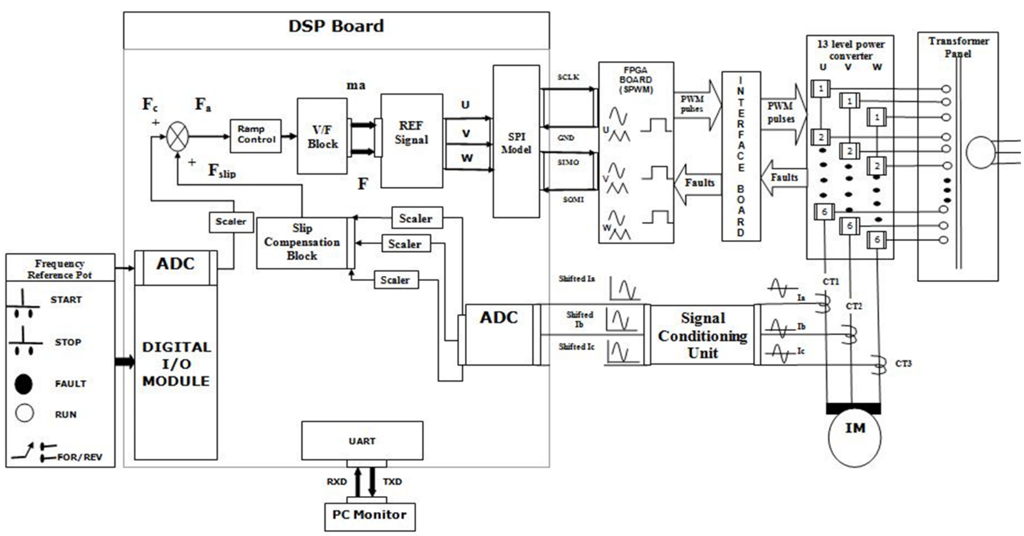

Figure 9. Control Block diagram of complete system

As shown in Fig.10, in advanced D.C. injection braking line-to-line voltage and stator currents are unidirectional and there is no back emf. And as in advance D.C. Injection Braking motor behaves as very weak generator there is no change in D.C. bus voltage.

Fig. 11, Fig. 12 and Fig. 13 represents the phase current when D.C. Braking is applied at 1200 rpm and 500rpm for various load conditions respectively by proposed techniques of the paper. Before applying D.C. braking base-block time of 200msec is given to de-magnetize the stator coils. After base-block time D.C. Braking applied for short period. It has been observed that the peak of injected current is reduced as load is increased. Also, a comparative analysis can be shown that in the proposed topology the effect of back emf is totally suppressed as compared to the previous IM drives. Hence current direction is purely unidirectional.

In Fig.14, speed characteristics of the IM drive is shown when D.C. Braking is injected at 1200 and 800 rpm respectively. It can be observed that the speed comes to zero in lesser time when D.C. is injected at 800 rpm than 1200 rpm. Tests have provided some amazing results. Motor have been able to stop from spins speeds in less than 0.5 seconds without noticeable motor heating. This same machine would take 40 to 50 seconds to coast to stop.

Lastly, in Table 6.1, a comparative observation has been shown between different D.C. braking schemes. It is clearly visible that the advanced D.C. injection brake system is better and more efficient than the rest braking schemes in terms of the amount of braking torque and the ability to stop motors with high inertia loads rapidly.

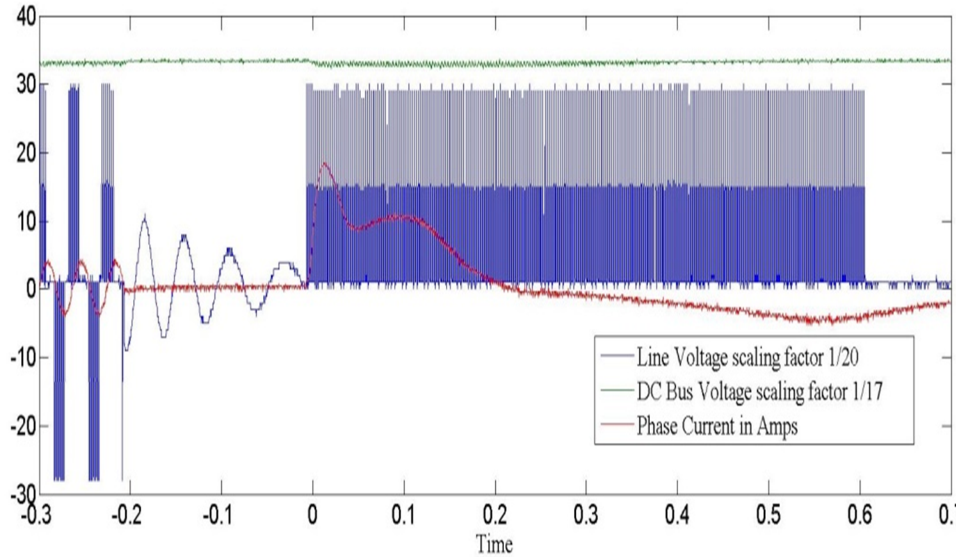

Figure 10. Line voltage, stator current and Bus voltage when applied advance D.C. Injection Braking

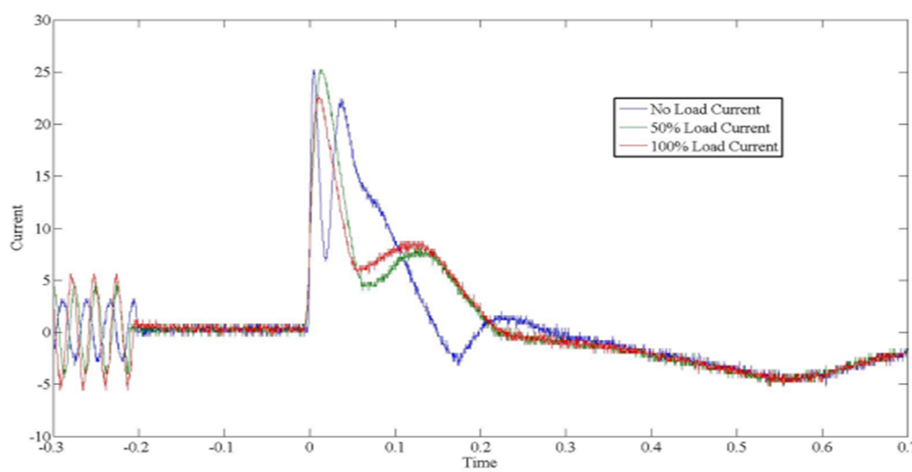

Figure 11. Stator current when applied advance D.C. Injection Braking at 1200 rpm

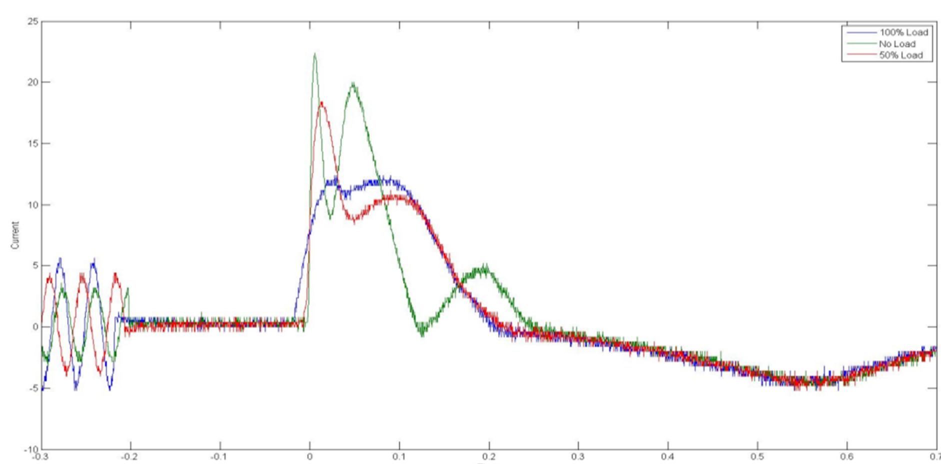

Figure 12. Stator current when applied advance D.C. Injection Braking at 800 rpm

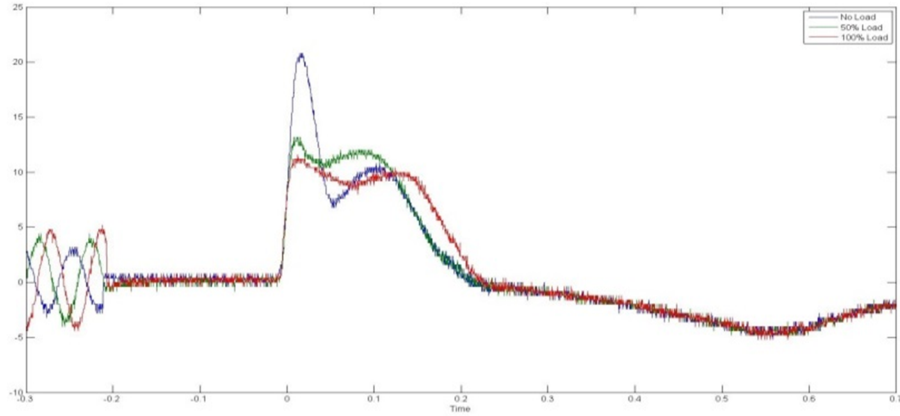

Figure 13. Stator current when applied advance D.C. Injection Braking at 500 rpm

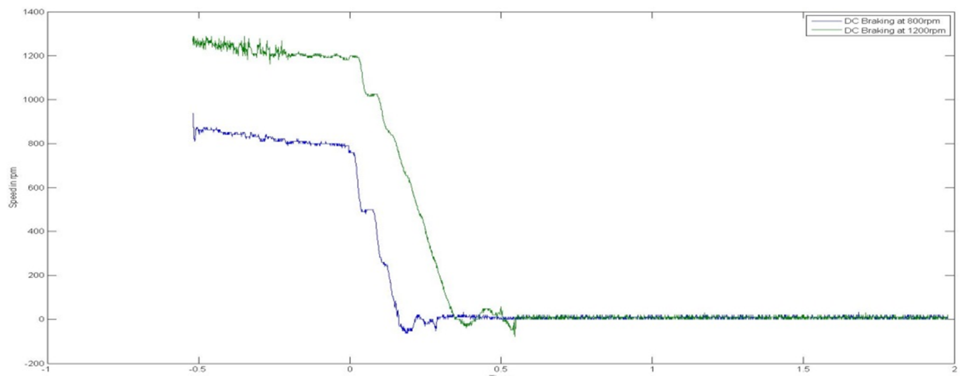

Figure 14. Speed-time curves when D.C. Braking applied at 1200rpm and 800rpm

Table 6.1. Comparison between regenerative/non-regenerative braking schemes in VFD

Parameters	D.C. Injection Braking	Dynamic Braking	Advanced D.C. Injection Braking	Flux Braking
Braking Type	Non-regenerative	Regenerative	Non- regenerative	Regenerative
Motor Heating	Upto 66%	100 to 150%	100%	Limited
Sink of Energy	Both Stator and Rotor	External Braking Resistor	Both Stator and Rotor	Stator (core)
Power Range	Low to Medium	High	High	Up to 7.5KW
High Inertia Load	Not Required	Not Required	Required	Not Required
Control Required	VFD	VFD+ Brake chopper + Resistor	VFD	VFD
Cost	0	Additional 20 to 30%	0	0

CONCLUSION

In this paper a method has been described for providing occasional braking torque from a non-regenerative multilevel VFD, without additional power circuits. The method has been shown to give significantly greater braking torque per ampere than D.C. injection braking in case of any medium voltage (MV) drive. A possible implementation has been presented, and supported with experimental results on low-voltage. The distinguished features of the proposed scheme are fast start of braking operation (approx. 200ms) and braking torque and braking time-out separately adjustable, requiring no external braking contactors. The most important advantage of the proposed technique is that no D.C. bus overshoot occurs during braking. Moreover, currents in all the phases are perfectly. Performance of advance D.C. braking has been compared to other recently-proposed methods. Proposed technique is not the answer for all application. However, it is a very cost-effective method for stopping high-inertia loads, even in the order of five times motor inertia. Proposed method offers slightly higher deceleration time when compared with dynamic braking but offer many advantages in many applications that require occasional braking. Efforts have been made in this paper to deal with the growing commercial market and industrial demand for high power MV drives with efficient and fast controlled braking system.

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